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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,935	11/18/2003	Kazuhiro Maeda	1035-483	3704

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EXAMINER	
EISEN, ALEXANDER	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 07/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/714,935	MAEDA ET AL.	
	Examiner	Art Unit	
	Alexander Eisen	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5 and 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujitani, JP 02-312099.

With respect to claims 1 and 8 Fujitani discloses a shift register block (FIG. 1) comprising at least one system of a shift register constituted of a plurality of unit circuits (D-flip-flops FF1-FF3) in a form of cascade connection and outputting an input signal (at nodes 1-3) in response to a clock signal CK, the shift register sequentially outputting a selection signal from output-stages (Q-outputs of flip-flops) constituted of the unit circuits, wherein the plurality of unit circuits are disposed with a unit circuit of a preceding output stage and a unit circuit of a following output stage being separated by a circuit different from the unit circuits (gates G1-G9).

As pertaining to claim 2,he shift the unit circuits are flip-flop circuits.

As pertaining to claims 3 and 5, the circuit different from the unit circuits is a processing circuit which uses output of one of the unit circuits constituting the shift register (note the gate G5 using output Q of the preceding unit FF1).

As pertaining to claim 7, the shift register block includes signal paths for the shift registers of the respective systems, the signal path being provided separately for each of the shift registers of the respective systems on both sides of a circuit alignment constituted of the unit circuits of the shift registers of the respective systems.

As per claims 8 and 9, Fujitani also discloses a data signal line driving circuit comprising a sampling section for driving a plurality of data signal lines (Add1-Add3 in FIG. 1) by sampling (using switches/transistors Q1-Q3) image data (see the abstract) from an image signal according to a selection signal (from the nodes 1-3) sequentially outputted from a shift register block so as to transfer the image data to the data signal lines, wherein the shift register block comprises: at least one system of a shift register constituted of a plurality of unit circuits in a form of cascade connection and outputting an input signal in response to a clock signal, the shift register sequentially outputting a selection signal from output-stages constituted of the unit circuits, the plurality of unit circuits being disposed with a unit circuit of a preceding output stage and a unit circuit of a following output stage being separated by a circuit different from the unit circuits (see relevant discussion of claim 1 having similar limitations).

4. Claims 13-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Washio et al., (hereinafter Washio), JP 2001-135093.

In regard to claim 13 Washio discloses a display device (FIG. 2), comprising a plurality of data signal lines SL1 - SLn; a plurality of scanning signal lines GL1 – GLn intersecting with the data signal lines; pixels 16 provided for each pair of the data signal lines and the scanning signal lines; a scanning signal line driving circuit 13 for driving the scanning signal lines; and a data signal line driving circuit 14 comprising a sampling section 18 for driving a plurality of data

signal lines by sampling image data from an image signal according to a selection signal S1 – Sn sequentially outputted from a shift register block 1 so as to transfer the image data to the data signal lines, wherein the shift register block 1 of the data signal line driving circuit comprises at least one system 4 of a shift register constituted of a plurality of unit circuits SR-FF in a form of cascade connection and outputting an input signal in response to a clock signal, the shift register sequentially outputting a selection signal S from output-stages constituted of the unit circuits SR-FF, the plurality of unit circuits being disposed with a unit circuit of a preceding output stage and a unit circuit of a following output stage being separated by a circuit 24 different from the unit circuits.

As pertaining to claim 14, Washio further discloses that the data signal line driving circuit and the scanning signal line driving circuit are formed on a substrate on which the pixels are formed (FIGS. 15-16; paragraphs [0096-97].

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 4, 6 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujitani in view of Karube et al., (Karube), US 6,072,456.

With respect to claims 4 and 6 Fujitani does not teach that the circuit different from the unit circuits is a unit circuit constituting a shift register of a different system, or that the shift register block includes signal paths for the shift registers of the respective systems, the signal

path being provided separately for each of the shift registers of the respective systems on both sides of a circuit alignment constituted of the unit circuits of the shift registers of the respective systems.

With respect to claim 10 Fujitani does not disclose that the sampling section carries out sampling of image data of divided image signals which are generated by dividing the image signal according to an alignment order of the data signal lines, the sampling section simultaneously carrying out sampling of the image data of the divided image signals.

Karube, however, with regards to claims 4 and 6, teaches a circuit for shift register having separate shift registers disposed between other shift registers (see FIG. 2; SR13-SR43), wherein signal paths are provided separately for each shift register.

Also, as pertaining to claim 10, Karube teaches driving of a flat panel display, wherein an image signal is divided according to an alignment order of the data signal lines (SV1 – SV8 in FIG. 2) and a sampling section (shift registers SR13-SR43) sample divided video data simultaneously (col. 4, lines 9-17).

It would have been obvious to one of ordinary skill in the art at the time when the invention was made to employ the technique taught by Karube in the driving apparatus of Fujitani, because it would allow to obviate an adverse influence of parasitic capacitance (col. 2, lines 43-48).

7. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujitani.

Fujitani does not discloses specifically that the image data sampled by the shift register is either analog or digital image data, but it would have been obvious to one of ordinary skill in the art at the time when the invention was made that image data can be represented by either one of

them and it would not bring any unexpected result. 11. Fujitani further teaches that the circuit different from the unit circuits is made up of at least one of a waveform shaping circuit or decoder circuit (such as a combination of the gates G1-G3 for instance).

8. Claims 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Washio in view of Brownlow et al., (Brownlow), US 6,232,946 B1.

With respect to claims 15 and 16 Washio does not teach that the pixels, the data signal line driving circuit, and the scanning signal line driving circuit include active elements, respectively, each of which is made of a polysilicon thin film transistor.

Brownlow, on the other hand, does teach the use of polysilicon transistors for fabricating driver monolithically on a display substrate (col. 1, ll. 52-62). Therefore, it would have been obvious to one of ordinary skill in the art at the time when the invention was made that in view of Brownlow the data signal line driving circuit, and the scanning signal line driving circuit include active elements, respectively, each of which is made alternatively of a polysilicon thin film transistor.

As pertaining to claim 16, Washio further discloses that the active elements are formed on a glass substrate at a process temperature of not more than 600°C (paragraph [0121]).

Allowable Subject Matter

Conclusion

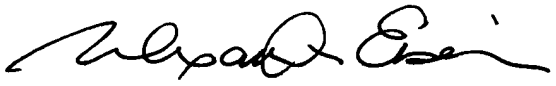
9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kawaguchi et al., US 5,602,561, discloses simultaneous sampling of divided video data.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander Eisen whose telephone number is (571) 272-7687. The examiner can normally be reached on M-F (9:00-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



Alexander Eisen
Primary Examiner
Art Unit 2629

28 June 2006